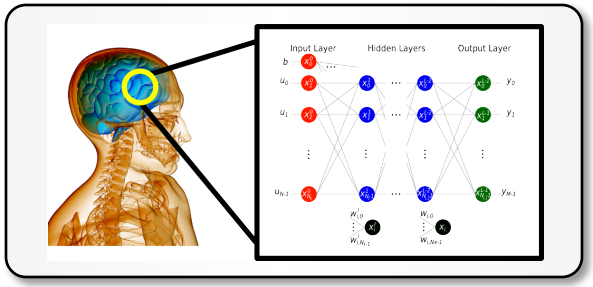
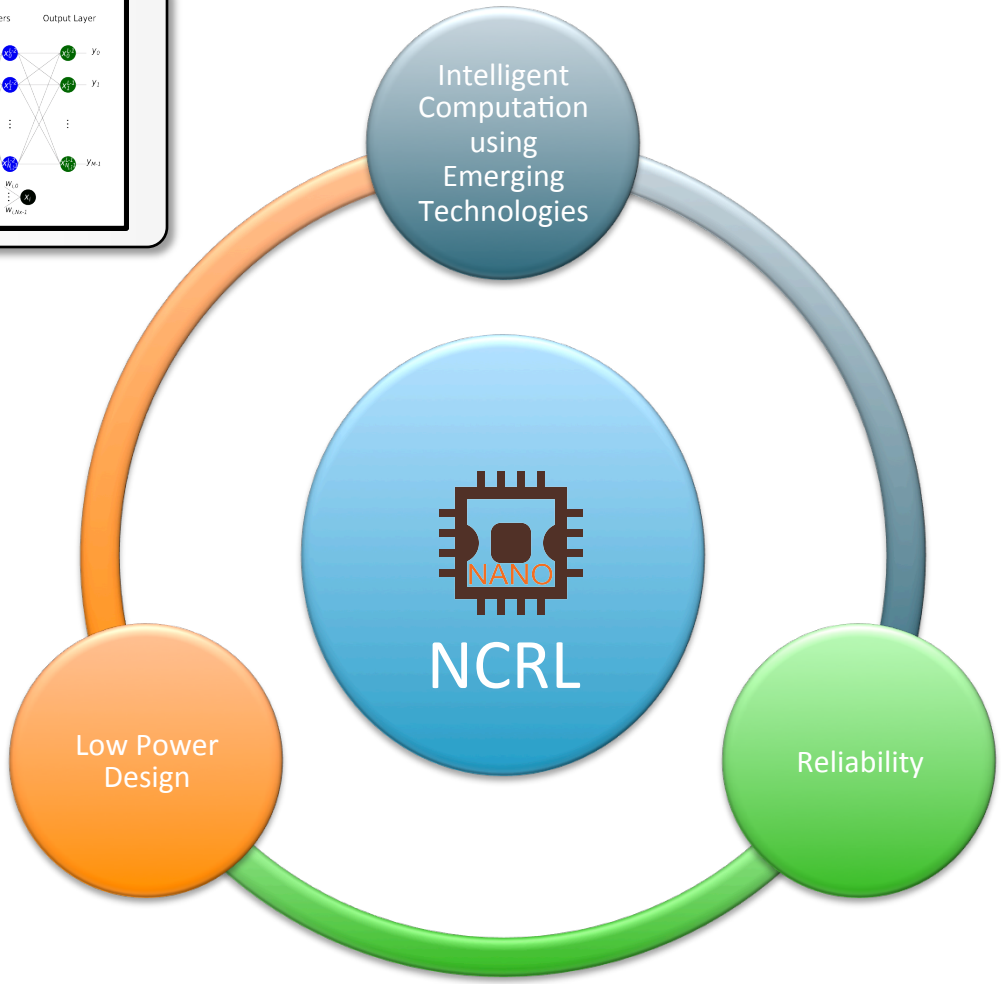
Towards Intelligent Computing with Neuromemristive Circuits and Systems

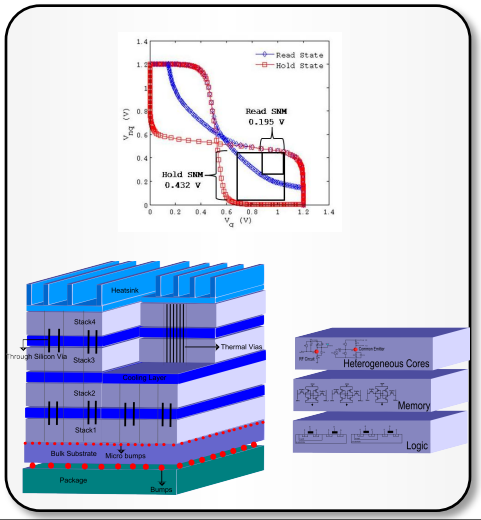
2014 NICE Workshop

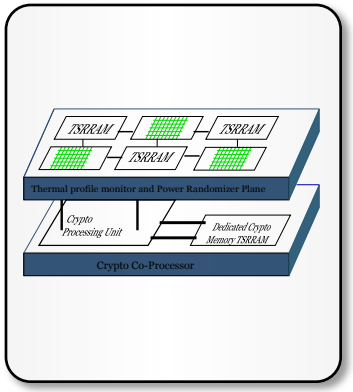
Dhireesha Kudithipudi, Ph.D.
Associate Professor
Nano Computing Research Lab
Department of Computer Engineering
Rochester Institute of Technology
Phone: 585-475-5085
E-mail: dxkeec@rit.edu; http://nano.ce.rit.edu

Nano Computing Research Lab

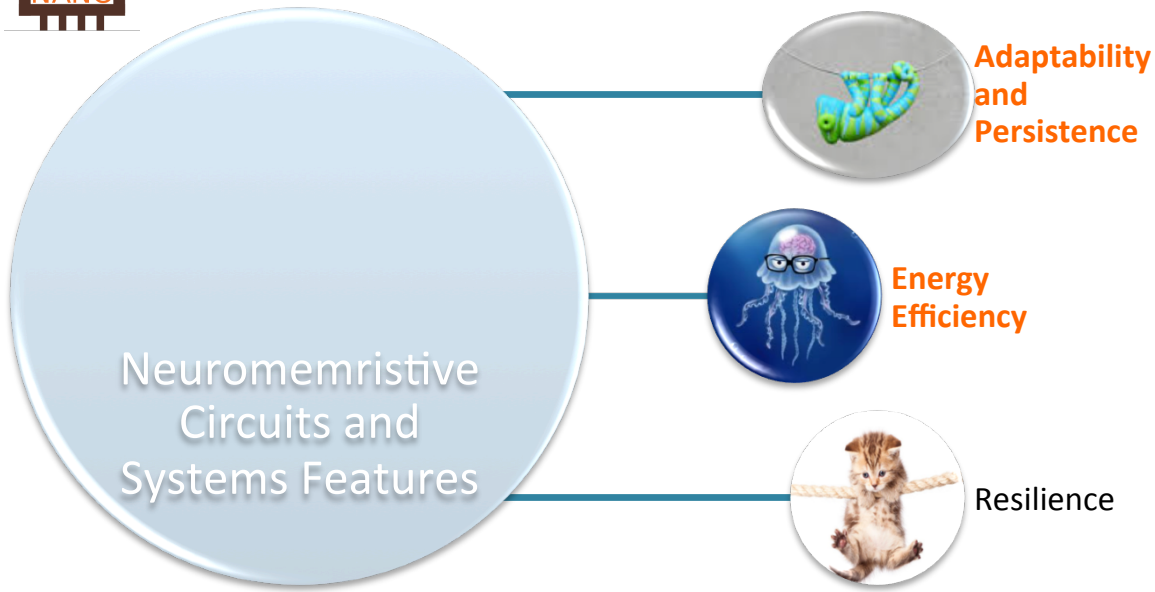








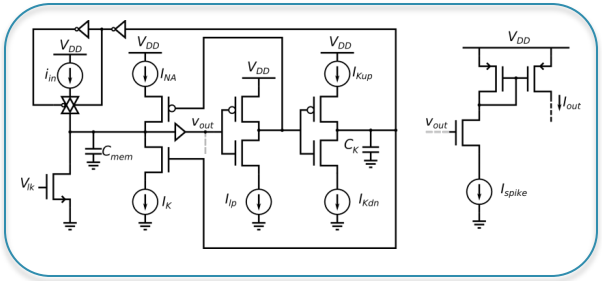
Enablers for Neuromemristive Hardware



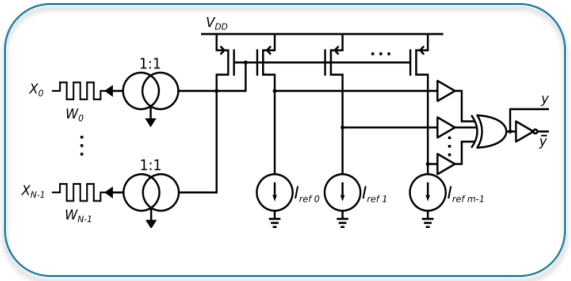
Neuromemristive Hardware (defn): A class of bio-inspired modular hardware that are implemented using CMOS-memristor technologies to create complex hierarchical computational architectures

Training	Activation Functions	Homeostasis
• Stochastic training algorithms • Adaptive Activation Functions	• Non-Monotonic • Heterogeneity	• Active and Passive Control of runtime parameters

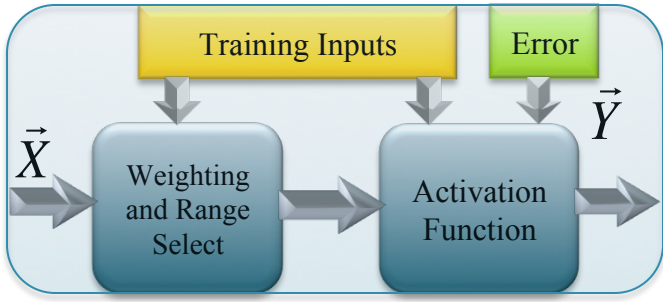
Single Neurons (Digital)



Spiking Neuron

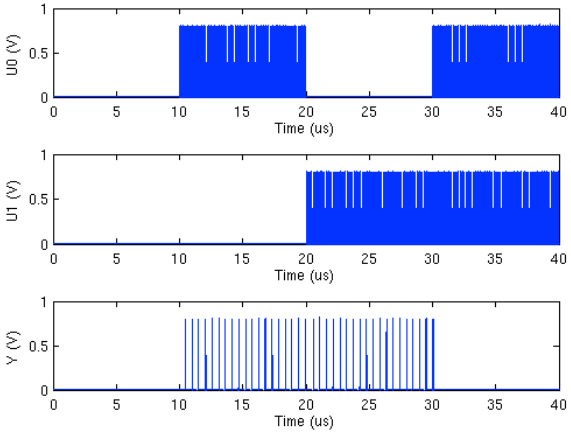


Non-Monotonic Neuron

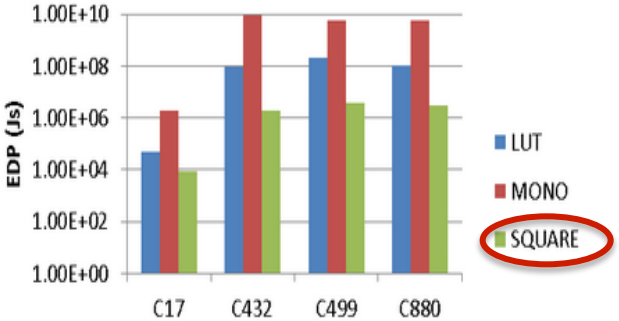


Adjustable Activation

Worst case power < 10nW



Edge Detection

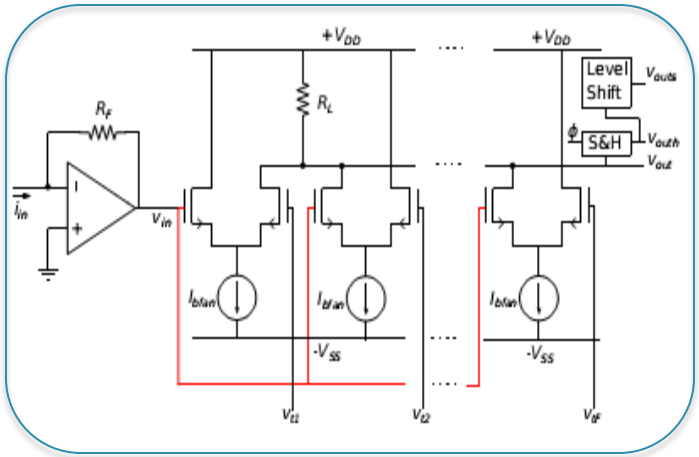


Energy-Delay Product

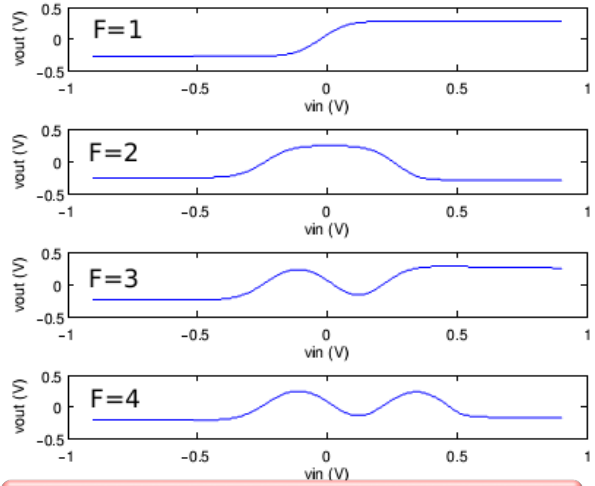
[1] M. Soltiz, D. Kudithipudi, C. Merkel, G. Rose, and R. Pino, "Memristor-based neural logic blocks for non-linearly separable functions," *IEEE Trans. Comp.*, vol. 62, no. 8, 2013,.
[2] *D.Kudithipudi, C. Merkel,* "Reconfigurable Memristor Fabrics for Heterogeneous Computing", in Advances in Neuromorphic Memristor Science & Applications, 2012
[3] M.Soltiz, D.Kudithipudi, G.Rose, RRAM-based Adaptive Neural Logic Block for Implementing Non-Linearly Separable Functions in a Single Layer," IEEE/ACM NANOARCH, 2012.

Single Neurons (Analog)

- Analog signals hold more information (higher info. Density)
- Suitable for applications that require continuous inputs
- Folding amplifier neurons generate periodic activation functions



Folding Amplifier Neuron



Sigmoid

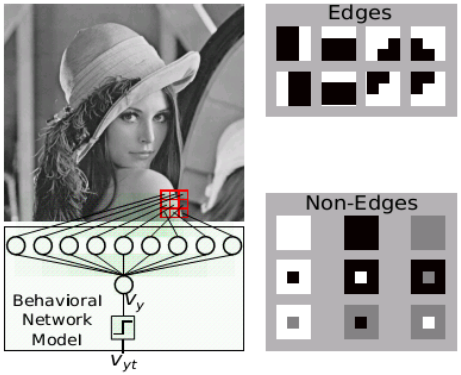
Radial Basis Function

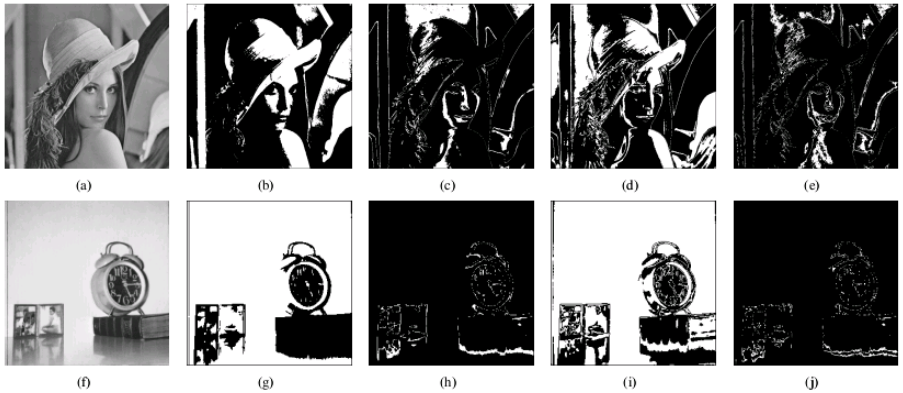
Activation Functions

[1] C. Merkel, D. Kudithipudi, and N. Sereni, "Periodic activation functions in analog CMOS/memrsistor hardware neural networks," *IJCNN*, 2013.

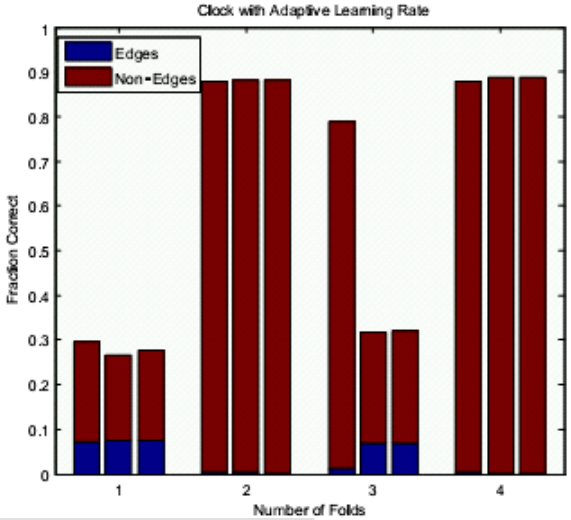
Feature Detection: Edge Detection

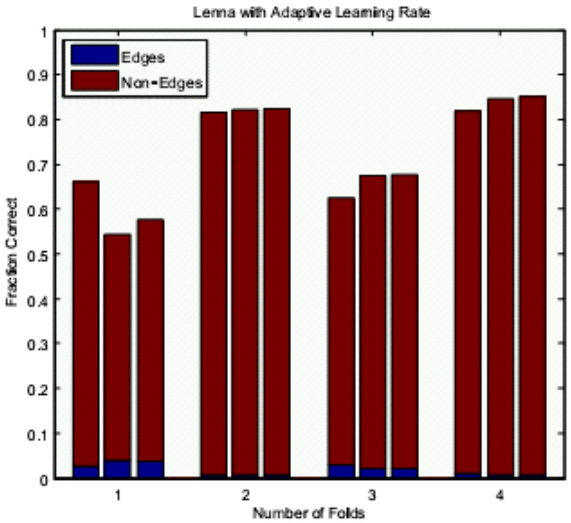
- Single-layer, single neuron network for image edge detection





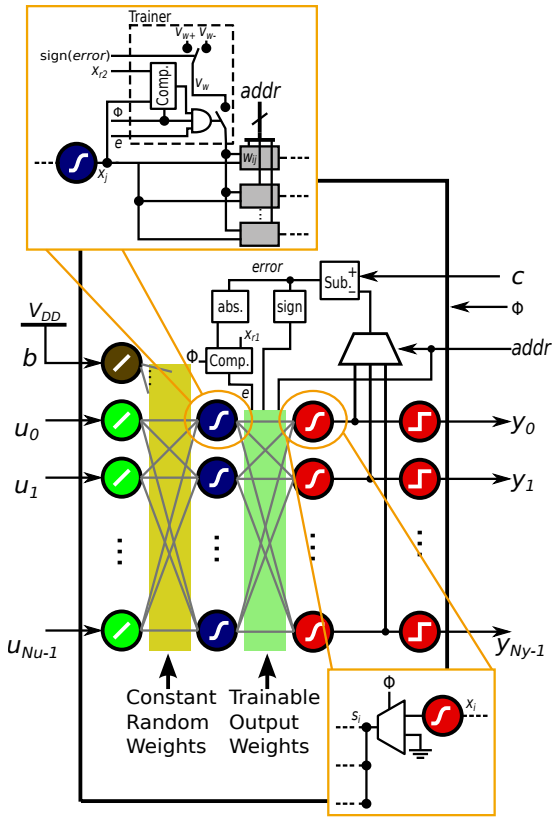
Can be used as low-level feature detectors in convolution networks.



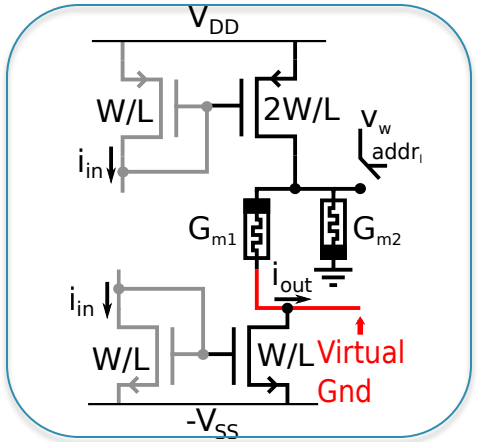


[1] C. Merkel, D. Kudithipudi, and N. Sereni, "Periodic activation functions in analog CMOS/memrsistor hardware neural networks," *IJCNN*, 2013.

Neuromemristive Networks



Extreme Learning Machine

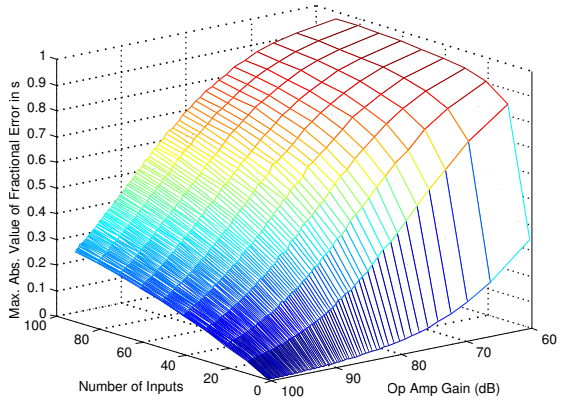


Synapse

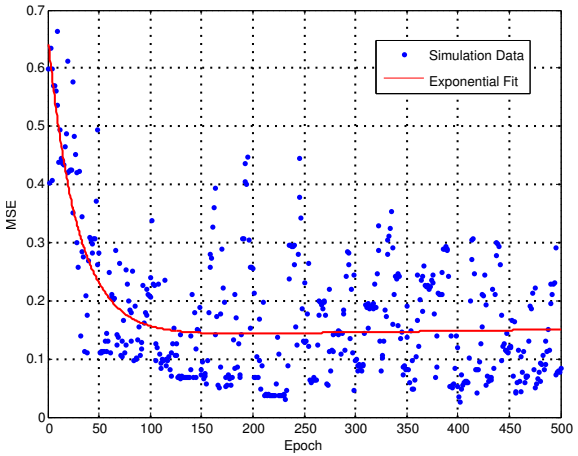
$$P\left(\frac{|\Delta w_{i,j}|}{\alpha}\right) = \beta\left(1, x_j\left|x_{i\exp} - x_i\right|\right)$$

$$\mathrm{sign}\left(\Delta t w_{i,j}\right) = \mathrm{sign}\left(x_{i\exp} - x_i\right)$$

Stochastic Training



Op Amp Gain Requirement

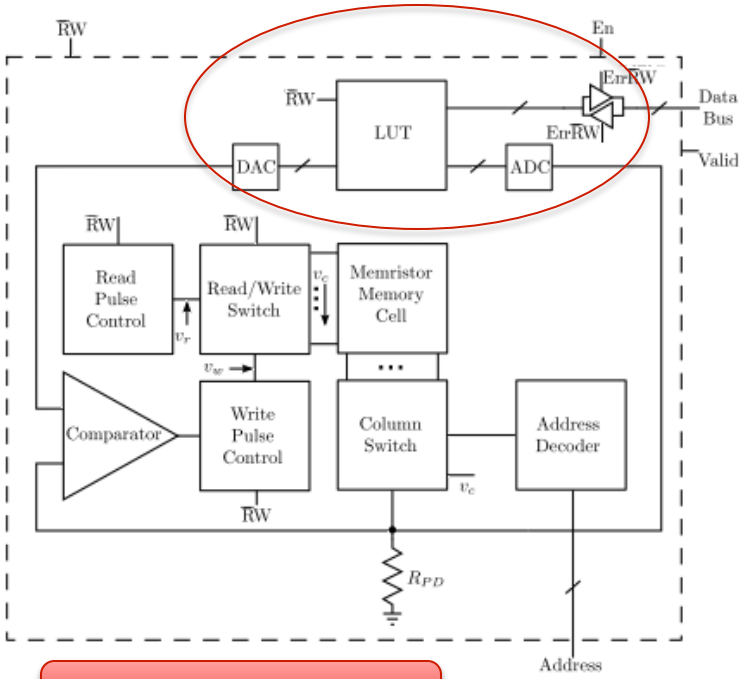


XOR Learning Curve

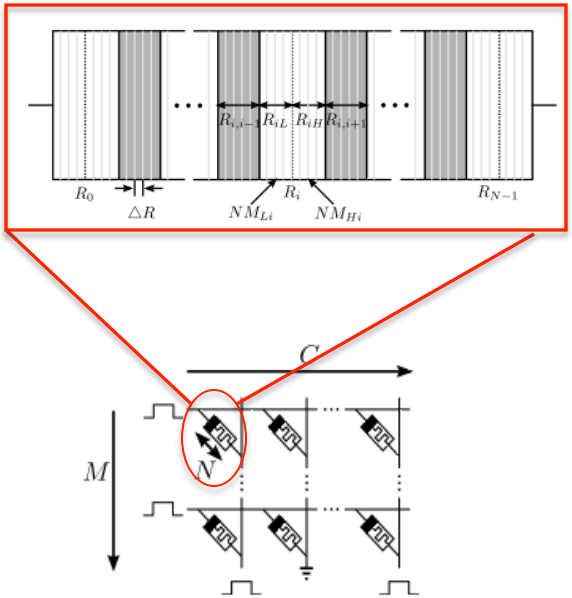
[1] C. Merkel, D. Kudithipudi, "A current-mode CMOS/memristor hybrid implementation of an extreme learning machine," *GLSVLSI*, 2014.

Reconfigurable Memory Density

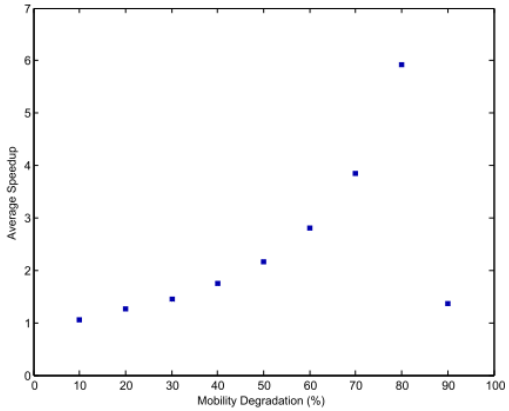
- Allows application to choose optimal memory density



Reconfigurable RRAM

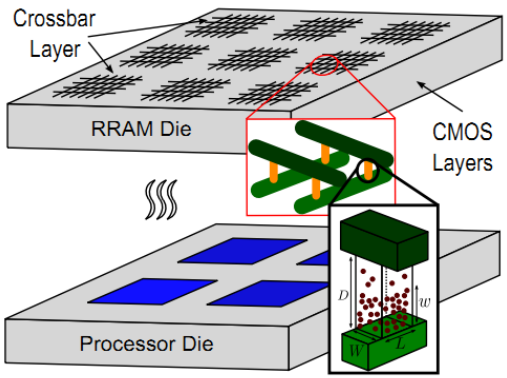


Combining Multiple Memristors Improves Write Speed

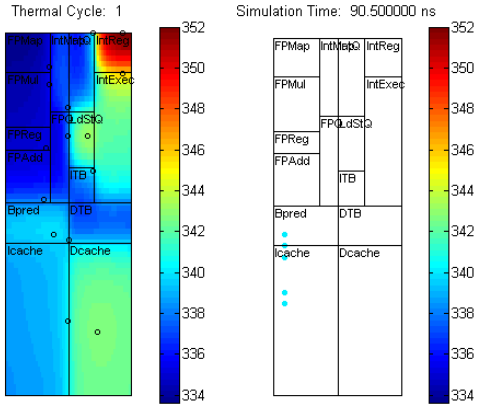


[1] C. Merkel, N. Nagpal, S. Mandalapu, D. Kudithipudi, "Reconfigurable N-level memristor memory design," *IJCNN*, 2011.

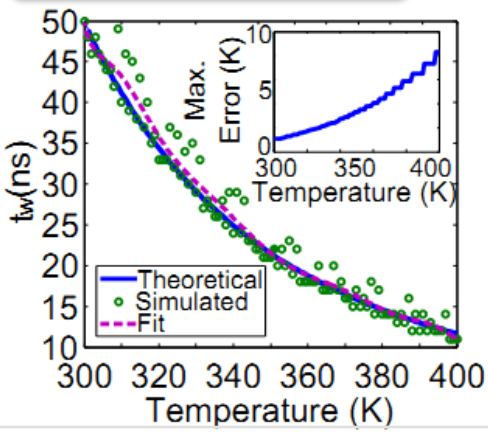
Homeostasis: Passive Control

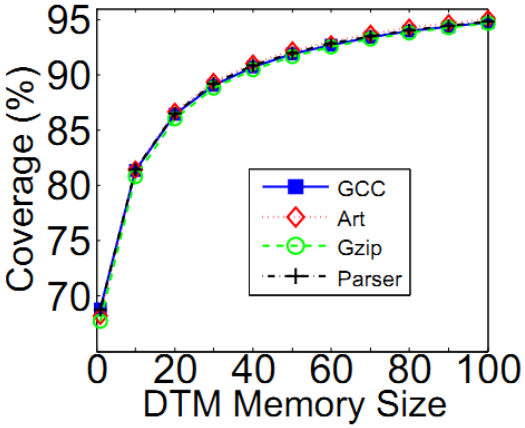


- ✓ Stabilize the temperature to mitigate the drift of weight states in a neuromemristive network
- ✓ Maximize energy efficiency.



3D Test Platform

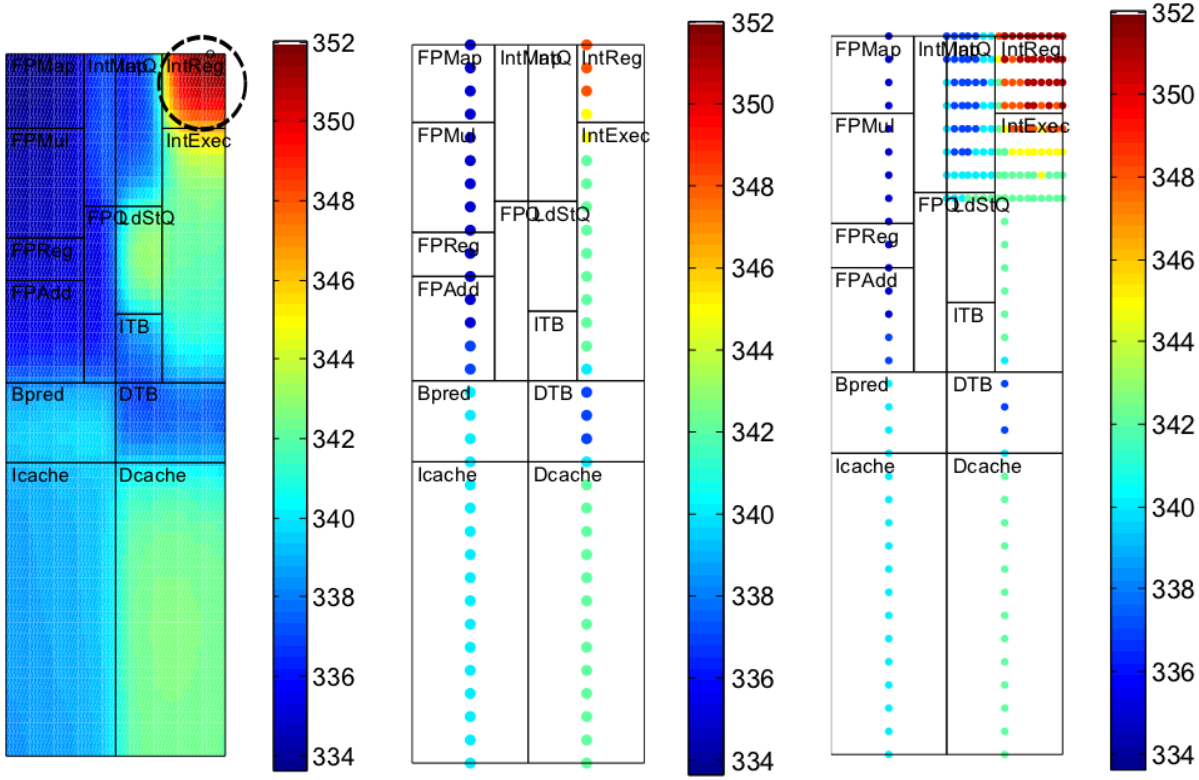


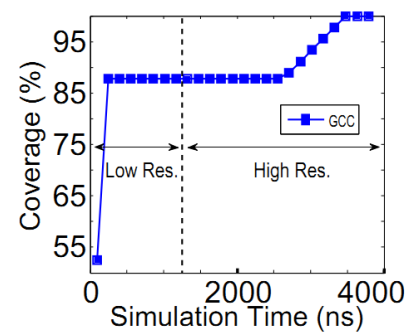


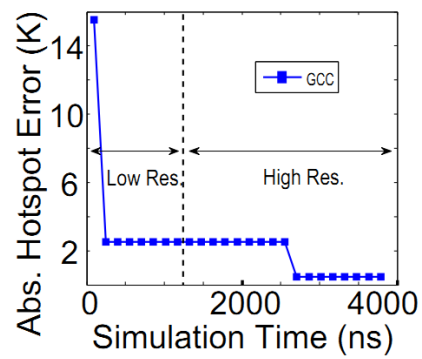
Passive Control

[1] C. E. Merkel and D. Kudithipudi, "Towards thermal profiling in CMOS/memristor hybrid RRAM architectures," VLSID, Jan., 2012.
[2] C. Merkel and D. Kudithipudi, "Temperature sending RRAM architecture for 3-D ICs," *IEEE Transactions on VLSI*, 2013.
3] C. Merkel and D. Kudithipudi. "Thermal management apparatuses with temperature sensing resistive random access memory devices and methods thereof." U.S. Patent 13/536,675.

Homeostasis: Active Control



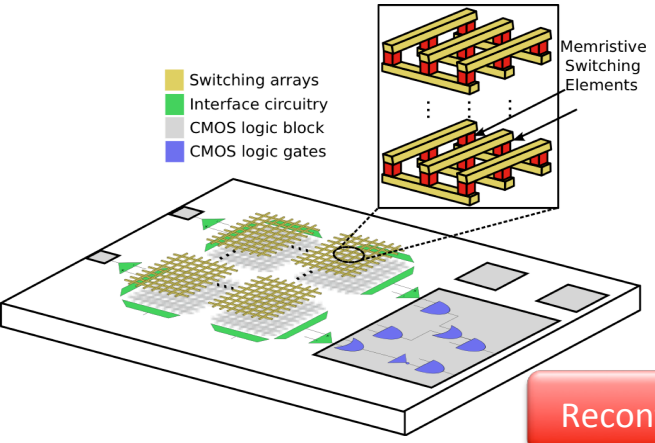




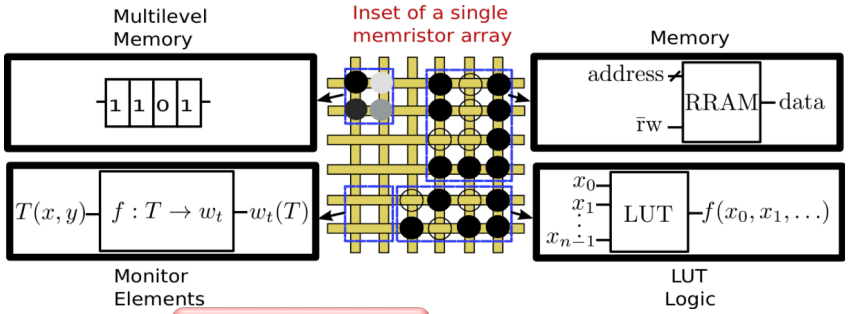
Active Control

[1] C. E. Merkel and D. Kudithipudi., "Towards thermal profiling in CMOS/memristor hybrid RRAM architectures," *VLSID*, Jan., 2012.
[2] C. Merkel and D. Kudithipudi, "Temperature sending RRAM architecture for 3-D ICs," *IEEE Transactions on VLSI*, 2013.

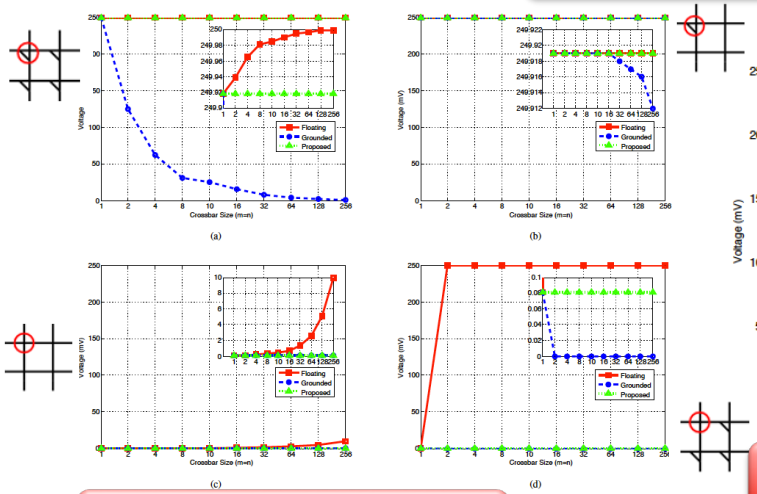
Augmenting Neuromemristive Systems with Reconfigurable Architectures



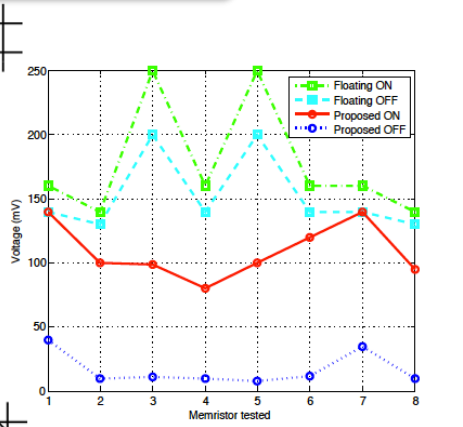
Reconfigurable Platform



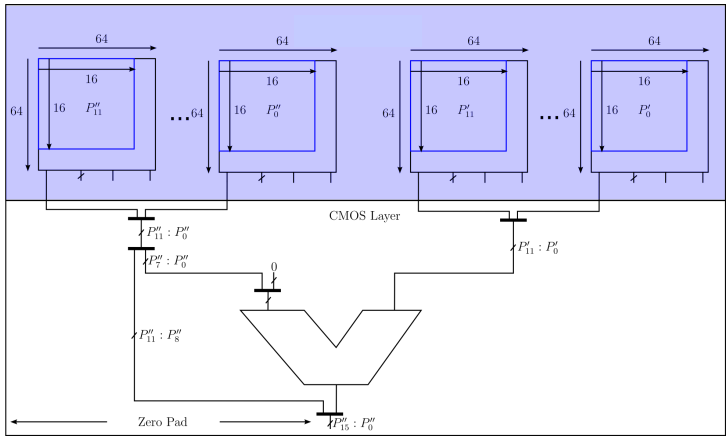
Flexibility



Sneak Path Mitigation



Experimental Validation



Constant Coefficient Multiplier

D. Kudithipudi, "FlexiMem: Reconfigurable Fabrics with Crossbars", AFRL Tech Report, 2011

Enablers for Neuromemristive Hardware

Neuromemristive Circuits and Systems Features

Adaptability and Persistence

Energy Efficiency

Resilience

Variation and Noise Tolerance

- Ratiometric Design
- Hardware in the loop training

Self-Healing

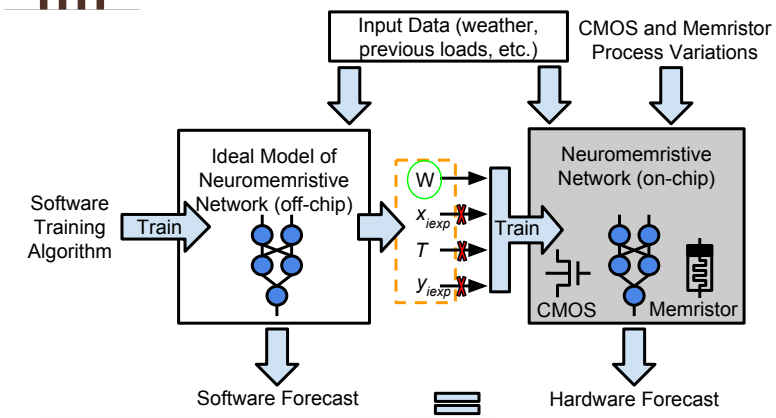
- Functionality Remapping
- Dynamic tuning of device

Process Variations of Primitives

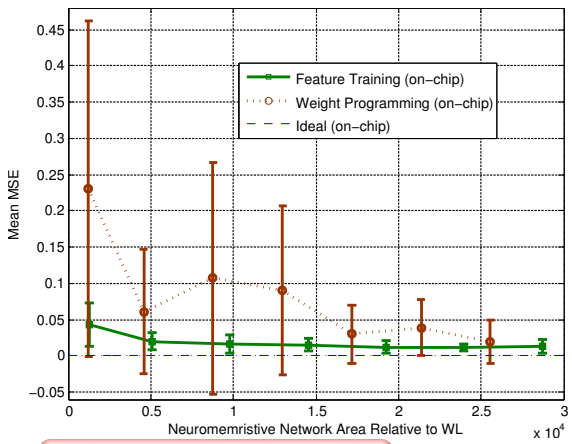
Circuit/Device	Variation
Constant Current Mirror	$\sigma(\Delta I_d) = \frac{I_d}{\sqrt{WL}}\sqrt{A_{V_{t0}}^2\left(\frac{g_m}{I_d}\right)^2 + A_\beta^2}$
Signal Current Mirror	$\Delta i_d = \frac{\Delta\beta}{\beta} i_d - g_m \Delta V_{t0}$
Differential Amplifier	$\sigma(v_{os}) = \frac{1}{\sqrt{WL}}\sqrt{A_\beta^2\left(\frac{I_{max}}{g_m}\right)^2 + A_{V_{t0}}^2}$
CMOS Resistors	$3\sigma(R) = \pm 30\%$
CMOS Capacitors	$3\sigma(C) = \pm 30\%$
Memristor G_{mon} and G_{moff}	$3\sigma(G_{mon}) = 3\sigma(G_{moff}) \approx 7\%$
Memristor t_w	$\sigma \approx 10\%$

[1] C. E. Merkel and D. Kudithipudi., "Off-chip training of neuromemristive networks for load forecasting in smart grids," IEEE *TNNLS,* 2014 (preprint) .

Process Variation Tolerance

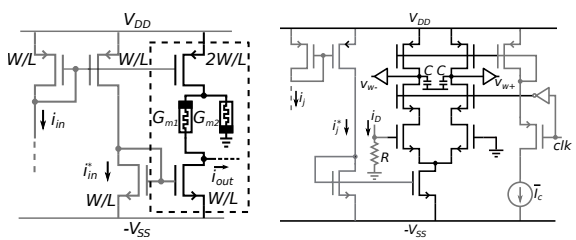


Off-Chip Training Framework

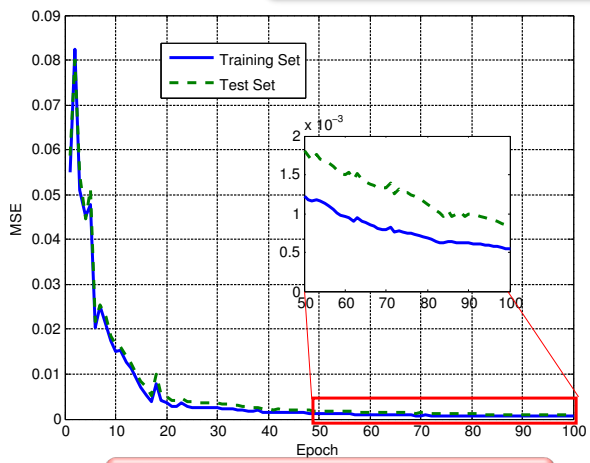


(Accuracy)$^{-1}$ vs Area

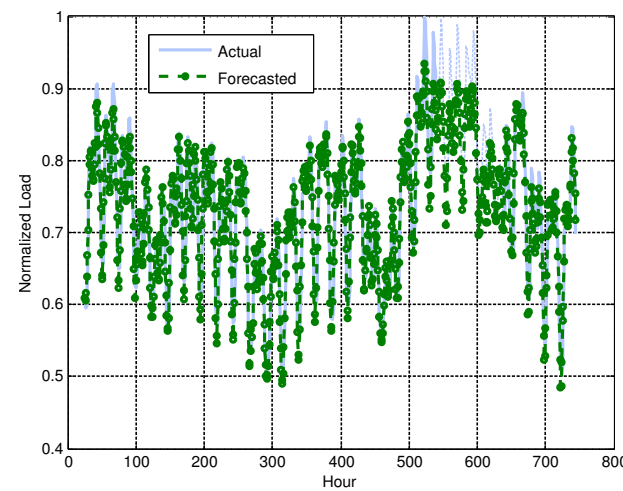
Accurate models are required for capturing the effect of process variations in the training process



Synapse and Training Hardware



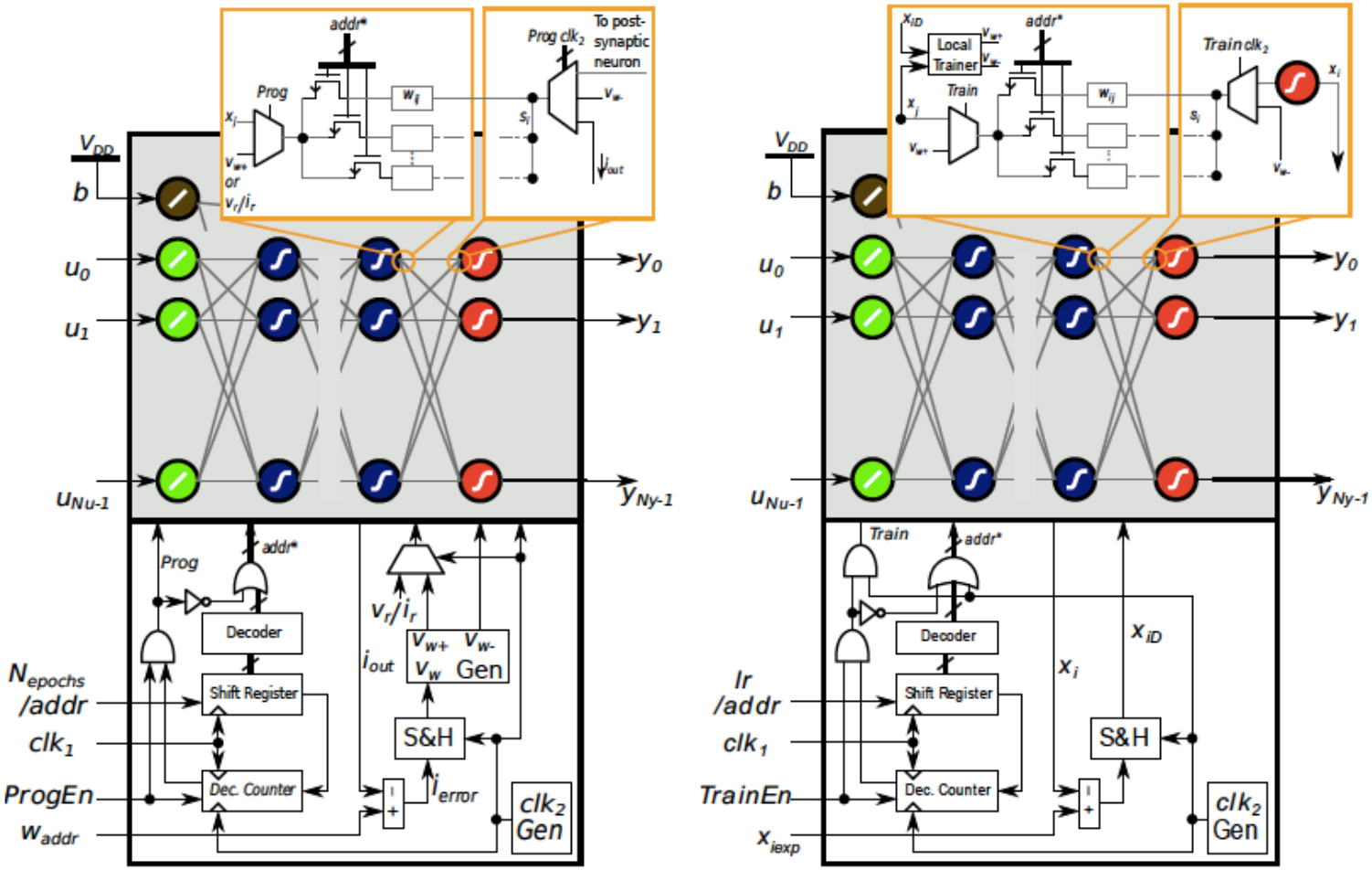
(Accuracy)$^{-1}$ vs training epoch



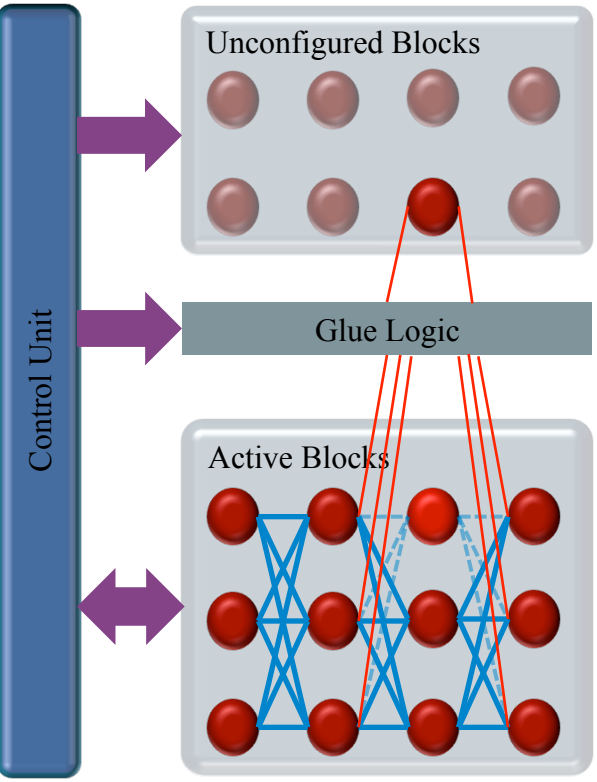
Forecasted Load Accuracy

[1] C. E. Merkel and D. Kudithipudi., "Off-chip training of neuromemristive networks for load forecasting in smart grids," IEEE *TNNLS,* 2014 .

Architecture Models

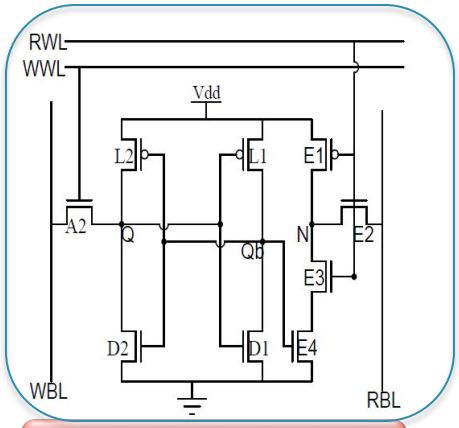


Reliability and Reconfigurability

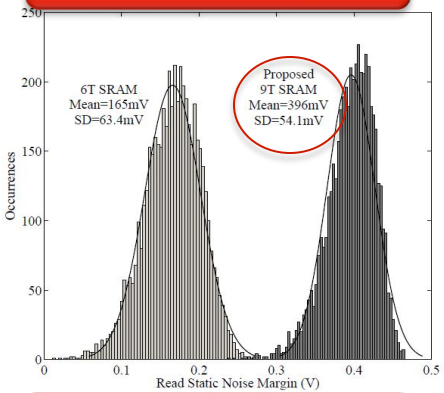


Runtime Reconfigurability Framework

- Enhance resilience by runtime remapping of the faulty/defect neuromemristive blocks
- Choose inherently variation tolerant CMOS hardware in the networks
- Stochastic signaling for soft error mitigation



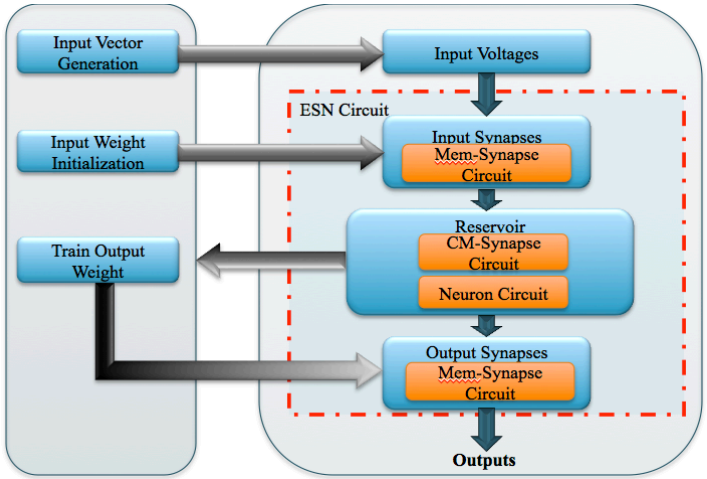
New SRAM design



Noise Margins

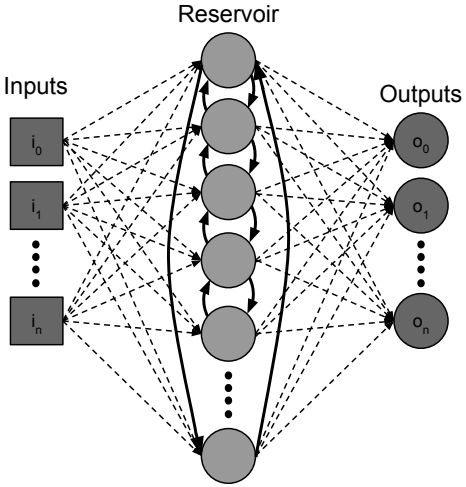
[1] M. Catanzaro and D. Kudithipudi, "Reconfigurable RRAM : A case study for reliability enhancement," IEEE *SOCC*' 12, 2012.
[2] S.H.Tavva, D. Kudithipudi, " Variation Tolerant 9T SRAM Design", ACM GLSVLSI'10, 2010

Neuromemristive Reservoirs

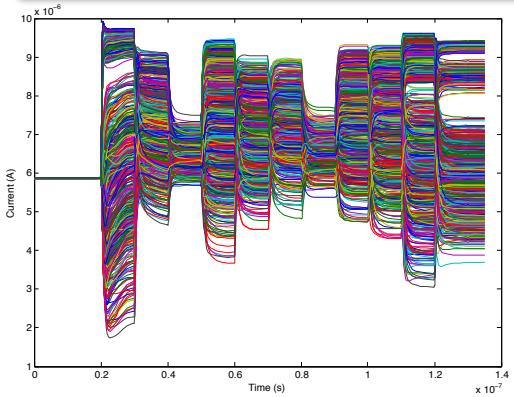


Hardware in the Loop Framework

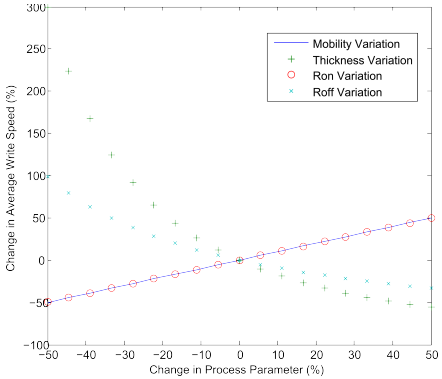
Works well for Classification problems



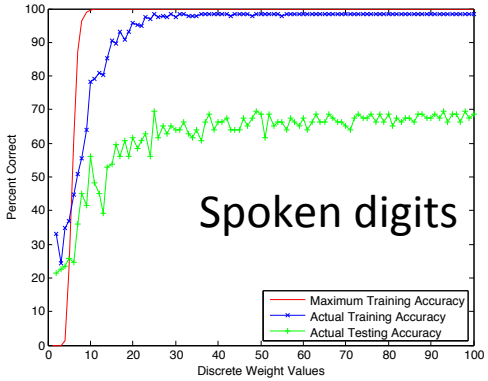
Reservoir Network



Reservoir Dynamics



Memristor Variations



Accuracy vs. Weight Precision

C.Donahue, D.Kudithipudi et.al., 2014

Few summary thoughts…

- Adaptability drives new complex systems
- Exploit device inherent properties
- Resilience in the design loop
- Reconfigurability with In-Memory Processing and sensing

- Not performance (speed)
- Not abstract them
- Not a design metric
- Not multiple layers

It doesn't matter how beautiful your theory is, it doesn't matter how smart you are. If it doesn't agree with experiment, it's wrong.

--Richard P. Feynman

Nano Computing Research Lab Team

Jet Propulsion Laboratory

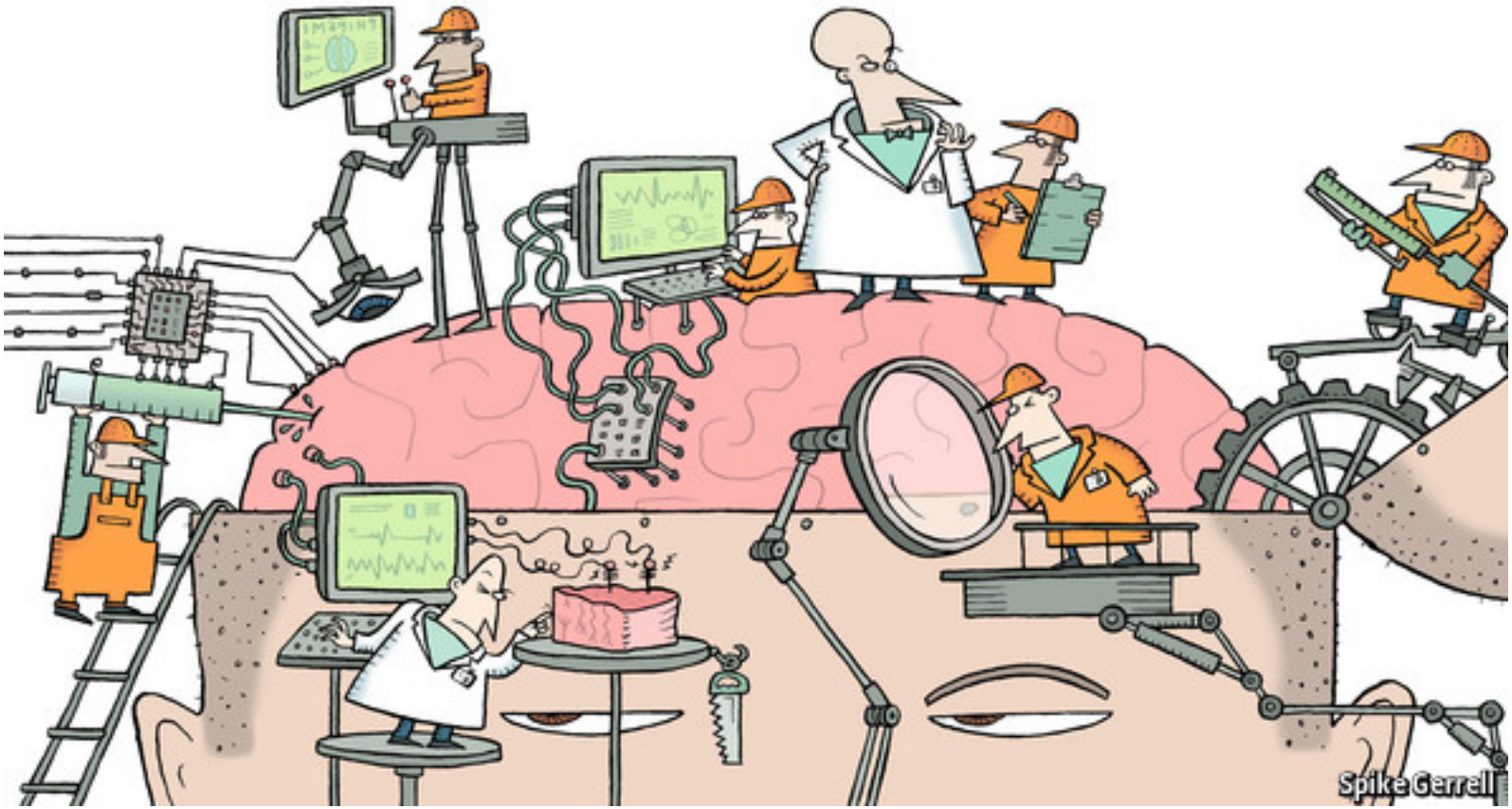
Acknowledgements

AIR FORCE RESEARCH LABORATORY

ARL

National Semiconductor

Thank You



Source: The Machine of a New Soul, Aug 2013, The Economist